The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 51

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte GERRIT J. KEESMAN

Appeal No. 2002-1426
Application No. 08/901,338

ON BRIEF

Before BARRETT, RUGGIERO, and BLANKENSHIP, Administrative Patent Judges.

BLANKENSHIP, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1-12 and 14, which are all the claims remaining in the application.

We reverse.

BACKGROUND

The invention relates to a method of compression for transmission of digital video signals between an encoder buffer and a decoder buffer. According to appellant, the method improves efficiency of decoder buffering by maintaining a relatively constant level of the decoder buffer fullness irrespective of signal bit rates. Representative claim 1 is reproduced below.

> 1. A method of compression for transmission of encoded digital video signals having a variable number of data bits per image frame, comprising the steps of:
>
> a) detecting a first bit rate of an encoded digital video signal bit stream;
>
> b) sequentially writing the encoded digital video signal bit stream in an encoder buffer at the first bit rate;
>
> c) deriving a second bit rate as a percentage of the first bit rate, which percentage changes inversely in relation to changes in the first bit rate; and
>
> d) reading the encoded digital video bit stream out of the encoder buffer at the second bit rate; and transmitting the encoded digital video bit stream to a decoder buffer at the second bit rate.

The examiner relies on the following reference:

Kiriyama	5,561,466	Oct. 1, 1996 (filed Jun. 23, 1994)

Claims 1-12 and 14 stand rejected under 35 U.S.C. § 102 as being anticipated by Kiriyama.

We refer to the Final Rejection (mailed Nov. 1, 2000) and the Examiner's Answer (mailed Jun. 19, 2001) for a statement of the examiner's position and to the Brief (filed

Apr. 3, 2001) and the Reply Brief (filed Aug. 22, 2001) for appellant's position with respect to the claims which stand rejected.

OPINION

Claims 1-12 and 14 are rejected under 35 U.S.C. § 102 as being anticipated by Kiriyama. Claims 1, 5, and 12 are independent.

Appellant argues that Kiriyama fails to disclose sequentially writing an encoded digital video signal bit stream in an encoder buffer at a first bit rate, and deriving a second bit rate as a percentage of the first bit rate, "which percentage changes inversely in relation to changes in the first bit rate."

The Answer (at 3) refers to the Final Rejection and to Paper No. 42, which sets forth the statement of the rejection.[1] The rejection therein asserts that Kiriyama teaches "detecting a first bit rate of the encoded digital video signal bit stream" in column 6, and deriving a second bit rate in a percentage "inversely related" to changes in the first bit rate, also in column 6. Appellant argues (e.g., Brief at 4-5) that Kiriyama is directed to "constant delay" criteria for synchronizing audio and video, and fails to disclose the claimed relationship between the first and second bit rate.

Kiriyama at column 6 refers to the structure depicted in Figure 5 of the reference. For an anticipation rejection to stand, it would appear that the corresponding limitations

[1] "An examiner's answer should not refer, either directly or indirectly, to more than one prior Office action." MPEP § 1208, under the heading "ANSWER."

of the claims must refer to data written at a "first bit rate" into encoder buffer 39, and the reading of data at a "second bit rate" out of the same encoder buffer. As shown in Figure 5, delay detector 49 senses both the input and output to buffer 39. According to column 6 of Kiriyama, video encoder 37 produces the encoded video signal as a succession of video frame data, each including a unique word UW, a predetermined time slot TD, and an encoded video datum VD as a frame structure. Delay detector 49 detects the delay of the read out video data relative to the video frame data and produces delay information DL representative of the delay, which is transmitted to delay information multiplexer 51.

Column 13 and Figure 16 of Kiriyama provide details of delay detector 49.

> Referring to FIG. 16, the delay detector 49 comprises a first unique word detector (UW DETECT) 123 supplied from the video encoder 37 with the video frame data to detect the unique word in each of the video frame data to produce a first unique word detection signal. Reset to zero by this unique word detection signal, a timer counter (TIMER) 125 counts up a bit count in each of the video frame data to produce a count signal representative of the bit count. A second unique word detector 127 is supplied from the buffer memory 39 with the read out video data to detect the unique word in each of the read out video data and to produce a second unique word detection signal.
>
> The count signal is supplied to a latch circuit 129 to update from time to time its content to the bit count which the count signal currently indicates. The second unique word detection signal is delivered to the latch circuit 129 to latch the bit count to which the content is updated. The latch circuit 129 produces a latch circuit output signal representative of the bit count under consideration as the delay information.

Kiriyama col. 13, ll. 10-29. The information determined by delay detector 49 thus relates to time delay, rather than bit rates.

"Anticipation is established only when a single prior art reference discloses, expressly or under principles of inherency, each and every element of a claimed invention." RCA Corp. v. Applied Digital Data Sys., Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984). Since the rejection does not point out any teaching of the express requirements of the claims relating to bit rates, the rejection must be founded on the principles of inherency. Our reviewing court has set out clear standards for establishing inherency.

> To establish inherency, the extrinsic evidence "must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." "Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient."

In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) (citations omitted).

The examiner has not provided any supporting evidence (e.g., explanatory references), but appears to submit reasoning to show that Kiriyama necessarily discloses that which is claimed. However, as appellant notes in the Reply Brief, there is reason for confusion as to what the Answer purports to demonstrate. For example, equation (5) on page 7 is deemed to be in the "well recognizable form of a standard linear algebraic equation of y = mx + b...." Whether B0, B2, and B3 are presumed to be bit rates, or delays associated with bit rates, however, it is not apparent why B0 and B3 are taken to be variable, but B2 (in addition to THV and ADV) is taken to be constant.

Moreover, even if the equation were to show a slope of -2, and an "inverse relationship" (Answer at 8), the equation appears to relate to delays (see id. at 6), rather than to bit rates.

We have carefully considered the teachings of Kiriyama and the examiner's arguments in support of the rejection. However, we agree with appellant that the reference fails to support a finding of anticipation. We thus do not sustain the rejection under 35 U.S.C. § 102.

CONCLUSION

The rejection of claims 1-12 and 14 under 35 U.S.C. § 102 as being anticipated by Kiriyama is reversed.

REVERSED

LEE E. BARRETT
Administrative Patent Judge

JOSEPH F. RUGGIERO
Administrative Patent Judge

HOWARD B. BLANKENSHIP
Administrative Patent Judge

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